

Unbuffered Memory Module Data Sheet

MW512N4013U58

512 MBytes, PC3200 (400MHz) CL3 184 Pin DIMM

Description:

The **MW512N4013U58** is a 512 Megabyte Memory Module, organized as 64Mx64 bits DDR-SDRAM. It is composed by eight 64Mx8 DDR-SDRAMs ICs in TSOP package and one serial EEPROM for SPD (Serial Presence Detect), mounted on a JEDEC-Standard 184-pin DIMM (Dual In Line Memory Module) with golden contacts.

Features:

- 184-pin DIMM outline, unbuffered
- Double Data Rate architecture; two data transfers per clock cycle
- Internal pipelined double data rate (DDR) architecture, with two data accesses per clock cycle
- Uses 64Mx8 DDR-SDRAMs
- Differential clock inputs
- Programmable burst length: 2, 4 or 8
- Programmable CAS latency:
 - CL=3.0 @ 200MHz, 400MT/s
 - CL=2.5 @ 167MHz, 333MT/s
 - CL=2.0 @ 133MHz, 266MT/s
- EEPROM Serial Presence Detection (SPD)
- Bidirectional data strobe (DQS)
- Four internal device banks for concurrent operation
- 8192 refresh cycles/64ms (4 banks concurrent refresh)
- Auto precharge
- Auto-refresh and Self-refresh modes
- Row address A0-12
- Column address A0-9,11
- SSTL_2 Interface
- VDD = VDDQ = 2.6 V ± 0.1 V

Specification:

Symbol	AC Characteristic	Min.	Max.	Unit	
t _{CK}	CLK Cycle Time	CL=3.0	5	10	ns
		CL=2.5	6	13	ns
		CL=2.0	7.5	13	ns
t _{RC}	Row Cycle Time (Operation)	55	-	ns	
t _{RAS}	Row Active Time	40	70,000	ns	
t _{RFC}	Auto Refresh to Active / Auto Refresh command period	70	-	ns	

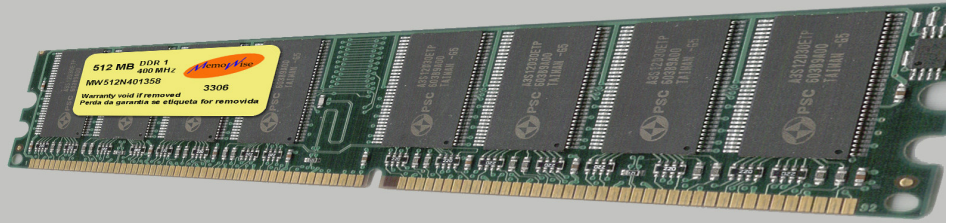
Ratings:

	Rating	Unit	Condition
Maximum Power Dissipation	12	W	Ta=25°C
Operating temperature	0 ~ 70	°C	
Storage temperature	-55 ~ 125	°C	

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Dimensions

All dimensions are in Inches; tolerance is $\pm 0.005''$ unless otherwise indicated

