

Unbuffered Memory Module Data Sheet

Imagem meramente ilustrativa

MW04GN1037UB8 / MW04GN1339UB8

4 GBytes, DDR3, PC3-8500 (1066 MHz) CL7 / PC3-10600 (1333 MHz) CL9, 240 Pin Unbuffered DIMM

Description:

MW04GN1037UB8 and **MW04GN1339UB8** are 4 Gigabyte Memory Modules, organized as 512Mx64 bits DDR3-SDRAM. Each module is composed by sixteen 256Mx8 DDR3-SDRAMs ICs in FBGA package forming two logical banks and one serial EEPROM for SPD (Serial Presence Detect), mounted on a JEDEC-Standard 240-pin DIMM (Dual In Line Memory Module) with golden contacts.

Features:

- 240-pin SO- DIMM outline, unbuffered;
- Dual Bank Memory Modules — Use 256Mx8 DDR3 SDRAMs;
- Double Data Rate architecture; two data transfers per clock cycle;
- On-Die Termination Control (ODT)
- Differential clock inputs
- Burst length (BL): 8 and 4 with Burst Chop (BC)
- Clock Cycle Time (t_{cx} avg):
 - MW04GN1037UB8: 1.87 ns @ CL = 7
 - MW04GN1339UB8: 1.5 ns @ CL = 9
- EEPROM Serial Presence Detection (SPD)
- Bidirectional, differential data strobe (DQS and /DQS)
- Eight internal device banks for concurrent operation;
- Refresh to Active (trFC): 107 ns (min);
- Auto precharge option for each burst access;
- Auto-refresh and Self-refresh modes;
- Row address A₀-A₁₄
- Column address A₀-A₉
- Bank address: BA₀~BA₂
- SSTL_15 Interface: VDD = 1.5 V ± 0.075 V;
- Refresh period (see note 6 below):
 - 0°C ≤ TC ≤ +85°C : 7.8 μs
 - +85°C < TC ≤ +95°C: 3.9 μs

DC Characteristics:

(TC=0°C to +85°C, VDD, VDDQ = 1.5V ± 0.075V)

Parameter (NOTE: As each bank may be in a different state, the data reflect the current consumption PER BANK)	Symbol	MW04GN1037UB8	MW04GN1339UB8	Unit	Notes
		max.	max.		
Operating Current (ACT=PRE)	IDD0	600	680	mA	
Operating Current (ACT-READ-PRE)	IDD1	760	800	mA	
Precharge Power Down Standby Current	IDD2P1	200	240	mA	Fast PD exit Slow PD exit
	IDD2P0	96	96	mA	
Precharge Quiet Standby Current	IDD2Q	240	280	mA	
Precharge Standby Current	IDD2N	256	296	mA	
Active Power-Down Current	IDD3P	240	280	mA	Always Fast exit
Active Standby Current	IDD3N	280	320	mA	
Operating Current	IDD4R	1120	1280	mA	Burst Read operating Burst Write operating
	IDD4W	1160	1320	mA	
Burst refresh Current	IDD5B	1520	1600	mA	

Recommended DC Operating Conditions:

(TC = 0°C to +85°C) 6

Parameter	Symbol	minimum	typical	maximum	Unit	Notes
Supply Voltage	VDD, VDDQ	1.425	1.5	1.575	V	1, 2, 3
	VSS	0	0	0	V	1
	VDDSPD	3.0	3.3	3.6	V	
Input Reference Voltage	VREFCA (DC)	0.49 x VDD	0.50 x VDD	0.51 x VDD	V	1, 4, 5
Input Reference Voltage for DQ	VREFDQ (DC)	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V	1, 4, 5

Notes:

1. DDR3 SDRAM Component Specification
2. Under all conditions VDDQ must be less than or equal to VDD.
3. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together
4. The AC peak noise on VREF may not allow VREF to deviate from VREF (DC) by more than ±1% VDD (for reference: approx. ±15 mV)
5. For reference: approx. VDD/2 ±15
6. When operating in the Range +85°C ~ +95°C (TC = temperature of the DRAM ICs case) the following must be observed:
 - a. Refresh commands must be issued at double frequency, thus tREF must be lowered to 3.9 μs
 - b. If Self-Refresh must be used, it is mandatory to either use Manual Self-Refresh with Extended Temperature Range Capability (MR2 bits [A6, A7] = [0, 1]) or Auto Self Refresh Mode must be enabled (MR2 bits [A6, A7] = [1, 0]).
7. tREFI depends on operating case temperature (TC)

AC Characteristics:

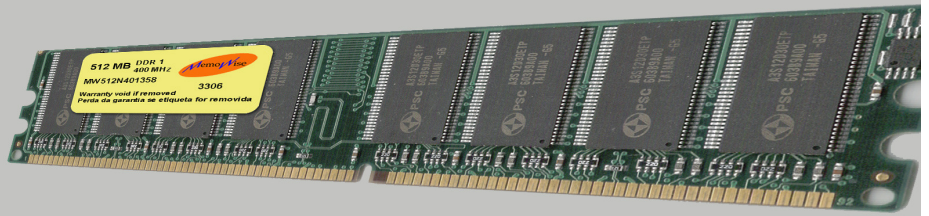
(TC=0°C to +85°C, VDD, VDDQ = 1.5V ± 0.075V, VSS, VSSQ = 0V)

Parameter	MW04GN1037UB8		MW04GN1339UB8		Unit (Notes)
	min.	max.	min.	max.	
tAA	13.91	20	13.91	20	ns
tWR	15	-	15	-	ns
tRCD	13.125	-	13.5	-	ns
tRRD (1K page)	7.5	-	6	-	ns
	4	-	4	-	nCK
tRRD (2K page)	10	-	7.5	-	ns
	4	-	4	-	nCK
tRP	13.125	-	13.5	-	ns
tRAS	37.5	9 x tREFI	36	9 x tREFI	ns (7)
tRC	50.625	-	49.5	-	ns
tRFC	160	70.200	160	70.200	ns
tWTR	7.5	-	7.5	-	ns
	4	-	4	-	nCK
tRTP	7.5	-	7.5	-	ns
	4	-	4	-	nCK
tREFI	-	7.8	-	7.8	μS (6, 7)
tREFI +85°C ≤ TC ≤ +95°C	-	3.9	-	3.9	μS (6, 7)

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Dimensions

All dimensions are in millimeters
Tolerance is $\pm 0.1\text{mm}$ unless otherwise indicated

